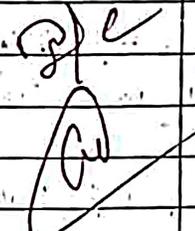


# I N D E X

Page No.

| Sr. No. | Experiment Description  | Experiment-Date | Submission Date | Remarks/Signatures |
|---------|---|-----------------|-----------------|--------------------|
| 1.      | Verify the open loop transfer characteristics of Op-amp using IC-741.   | 1 to 2          |                 |                    |
| 2.      | Design square wave generator using IC-741 and calculate the duty cycle of the generated waveform.                           | 3 to 5          |                 |                    |
| 3.      | Design an Astable Multi-vibrator using IC-555 timer and calculate the duty cycle and pulse width of the generated waveform. | 6 to 8          |                 |                    |

  
 Cu

# I . N . D . E . X

| Sr. No. | Experiment Description   | Experiment Date | Submission Date | Remarks/Signature |
|---------|--|-----------------|-----------------|-------------------|
| 4.      | Design a 2nd order active low pass filter, active high pass filter, active band pass filter using IC 741 op-amp. | 9-10-11         |                 |                   |
| 5.      | Calculate the lock range and capture range of PLL using IC-565.  | 12-10-14        |                 |                   |
| 6.      | Design of binary adder and subtractor.   | 15-10-18        |                 |                   |
| 7.      | Design of counter  | 19-10-22        |                 |                   |
| 8.      | Study of Multiplexer and demultiplexer/decoder.  | 23-10-26        |                 |                   |
| 9.      | Implementation of combination logical ckt.   | 27-10-28        |                 |                   |
| 10.     | Study of ADC and DAC.  | 29-10-20        |                 |                   |

AIM:- Operational Amplifiers (IC 741) characteristics and applications

Apparatus-

- op-amp (IC-741)

THEORY:-

The term operational amplifier is the full form of an op-amp and it is one kind of IC (integrated circuits). An op-amp is a DC-coupled high gain voltage amplifier with a differential i/p and a single o/p.

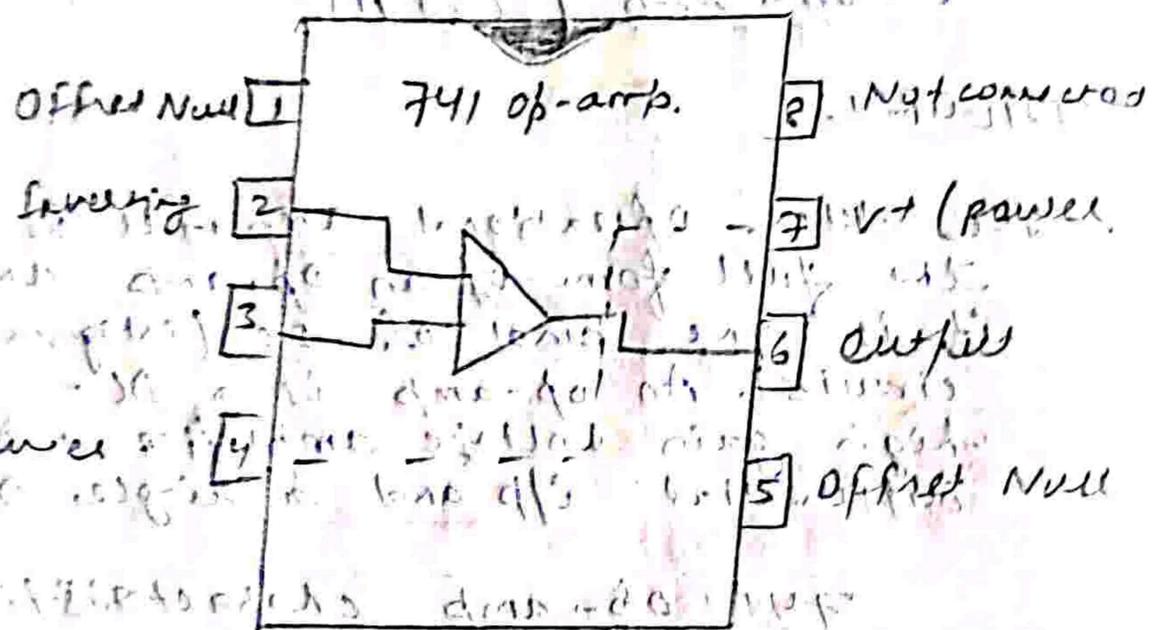
741 op-amp characteristics

The characteristics of the IC 741 operational amplifiers include the following

- The input impedance of the IC 741 op-amp is above 100 kilo-ohms.
- The o/p of the IC 741 op-amp is below 100 ohms.
- The frequency range of amplifier signals for IC 741 op-amp is from 0Hz - 1MHz

(unclear) circuit diagram

(unclear) diagram



741 Pin Diagram

The 741 op-amp is a single supply, voltage feedback, bipolar, general purpose operational amplifier. It is designed to be used in a wide range of applications. The pin diagram shows the connections for the power supply, input, and output.

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- The offset current and offset voltage of the IC 741 op-amp is low.
- The voltage gain of the IC-741 is about 2,00,000.

### 741 op-amp applications.

There are many el. circuits are built with IC 741 op-amp namely voltage follower, analog-digital converter, sample and hold ckt, the voltage to current and current to voltage converting.

- Variable audio frequency oscillator using IC-741 op-amp.
- IC 741 op-amp based adjustable ripple RPS.
- Audio mixture for four channels using IC-741 op-amp.
- IC-741 op-amp and LDR based automatic light operated switch.
- e-zoom thermometer using IC 741 op-amp.
- Microphone amplifier using IC 741 op-amp.
- Thermal touch switch using IC 741 op-amp.
- Conversion of V to F using IC 741 op-amp.

AIM:- Waveform Generation using op-amp. (IC)

APPARATUS:-

- op-amp IC 741 - 2 No.
- Bread board
- Capacitor 0.1  $\mu$ F - 3 No.
- RPS (0-30V) - 1 No.
- Resistors - 10k $\Omega$  - 2 No, 470k $\Omega$  - 1 No, 1k $\Omega$  - 3.
- connecting wires
- CRO (20MHz)

THEORY:-

RC oscillator is build using an amplifier and RC network in feedback. For any oscillator the two prime requirements to generate sustained and constant oscillations are -

(i) The total phase shift around loop must be 0° to 360° degrees.

(ii) The loop gain should be equal to unity.

- This known as "Barkhausen Criterion".

The circuit oscillates at a frequency,  $f = \frac{1}{2\pi RC\sqrt{6}}$

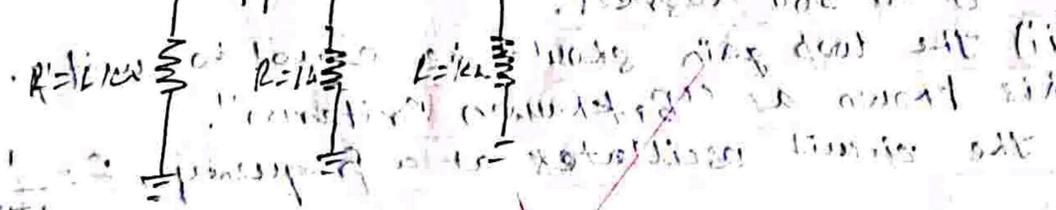
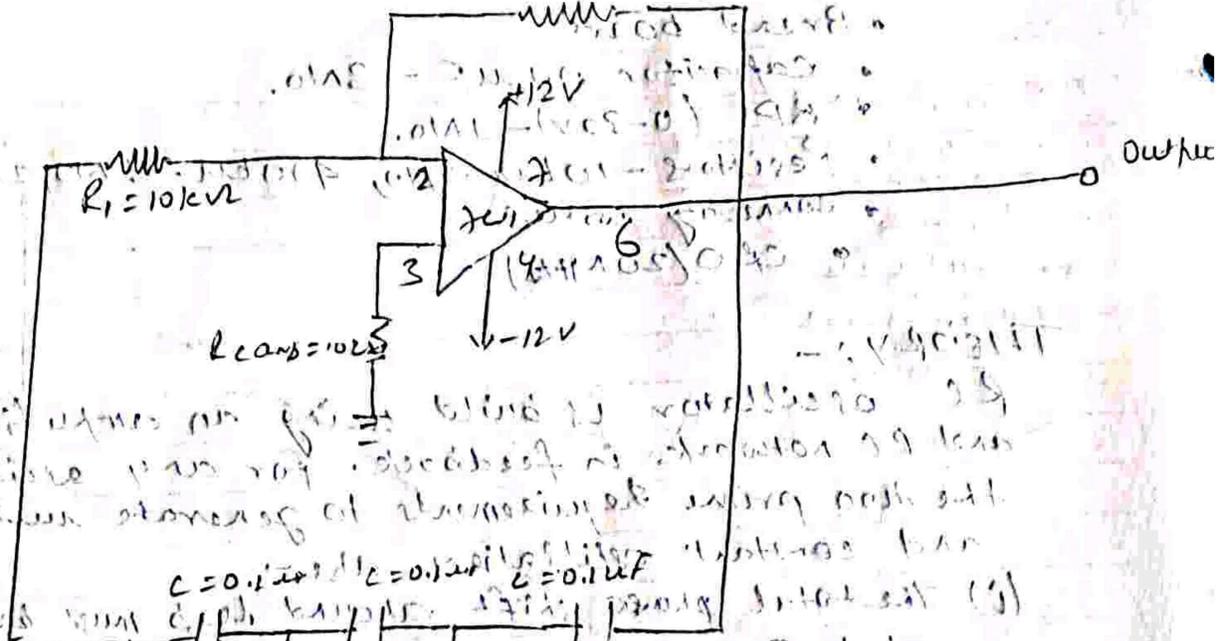
The common equation for the time period can be simplified as -

$$T = 2.1976 RC$$

The frequency can be determined by the equation,  $f = \frac{1}{T}$

Circuit diagrams:

Sine wave Generator: (RC phase shift oscillator)



The circuit is a phase shift oscillator. The feedback network consists of three RC stages. The first stage is a resistor  $R_1 = 10k\Omega$ . The second stage is a resistor  $R_2 = 1k\Omega$  in series with a capacitor  $C = 0.1\mu F$ . The third stage is a resistor  $R_3 = 1k\Omega$  in series with a capacitor  $C = 0.1\mu F$ . The output is taken from the op-amp's output terminal. A  $-12V$  supply is connected to the non-inverting input. The circuit is powered by a  $12V$  supply.

### PROCEDURE:-

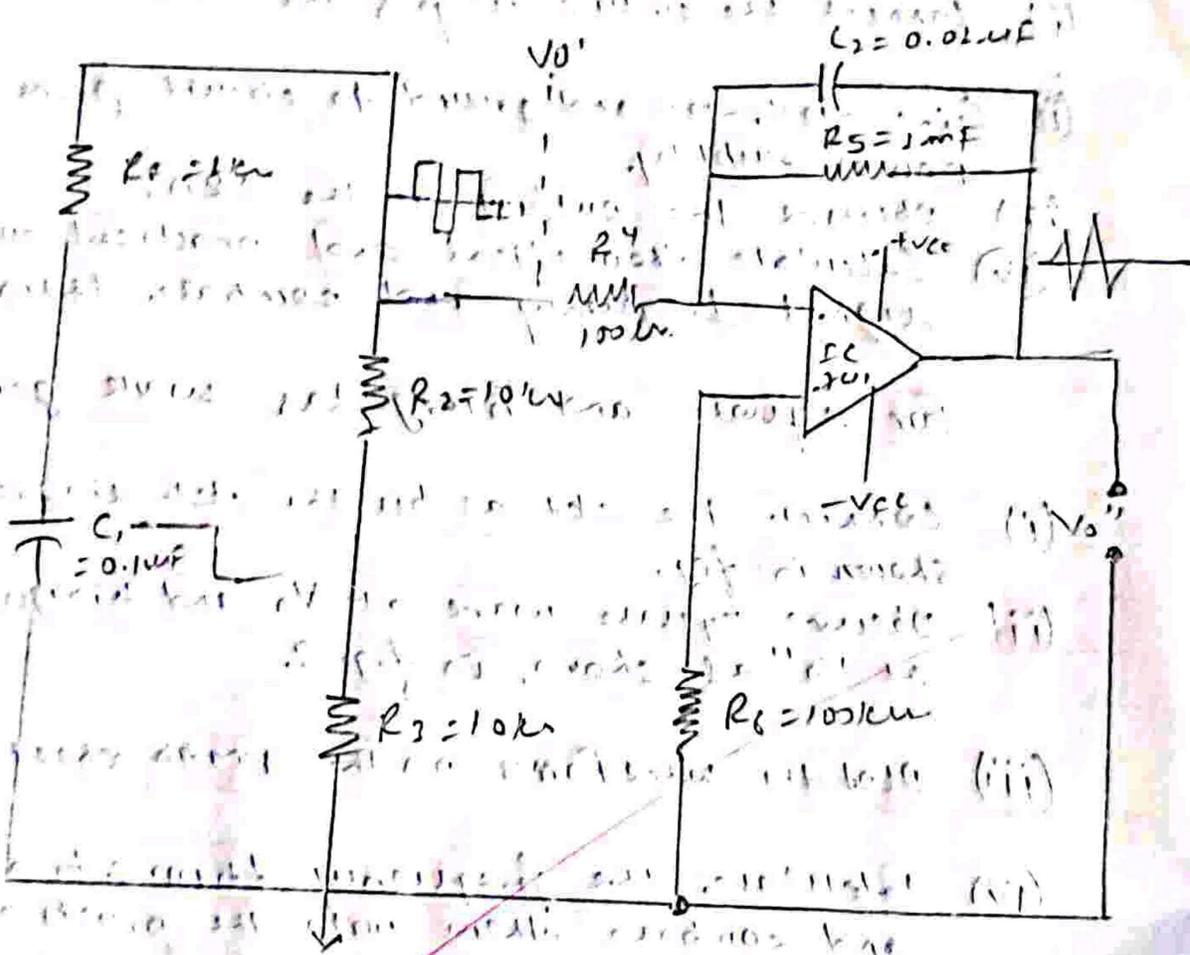
for sine wave generation

- (i) Connect the circuit as per the circuit diagram
- (ii) Give +12V, -12V and ground to circuit from power supply.
- (iii) Observe the output on the CRO.
- (iv) Calculate theoretical and practical output signal frequency and compare them.

for square and triangular wave generation

- (i) Connect the ckt as per the ckt diagram shown in fig.
- (ii) Observe square wave at  $V_0$  and triangular at  $V_0''$  as shown, in fig. 3.
- (iii) Plot the waveforms on the graph sheet.
- (iv) Calculate the frequency theoretically and compare them with the practical one.

# Square and Triangular Wave Generator



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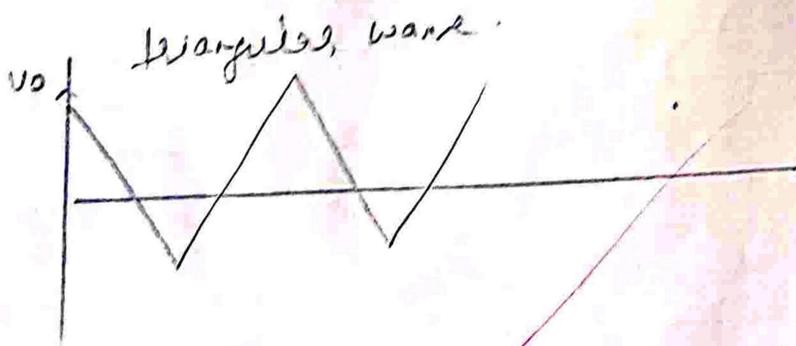
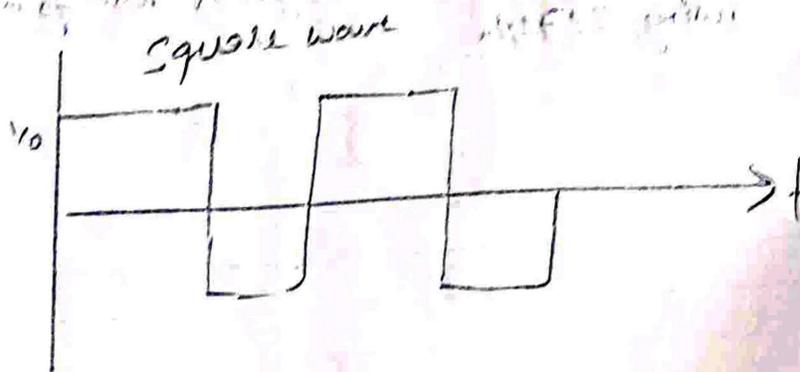
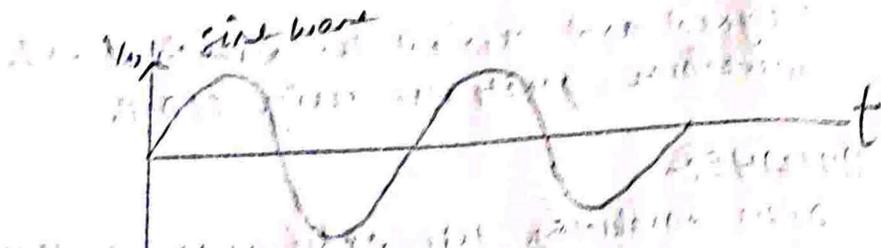
**RESULT :-**

Designed and verified the waveform of waveform generator using IC 741.

**OUTCOME :-**

After conducting this experiment, students are able to design and generate sine, square and triangular waveforms using IC 741.

# Expected waveforms:



AIM:- Applications of timer IC555.

THEORY:-

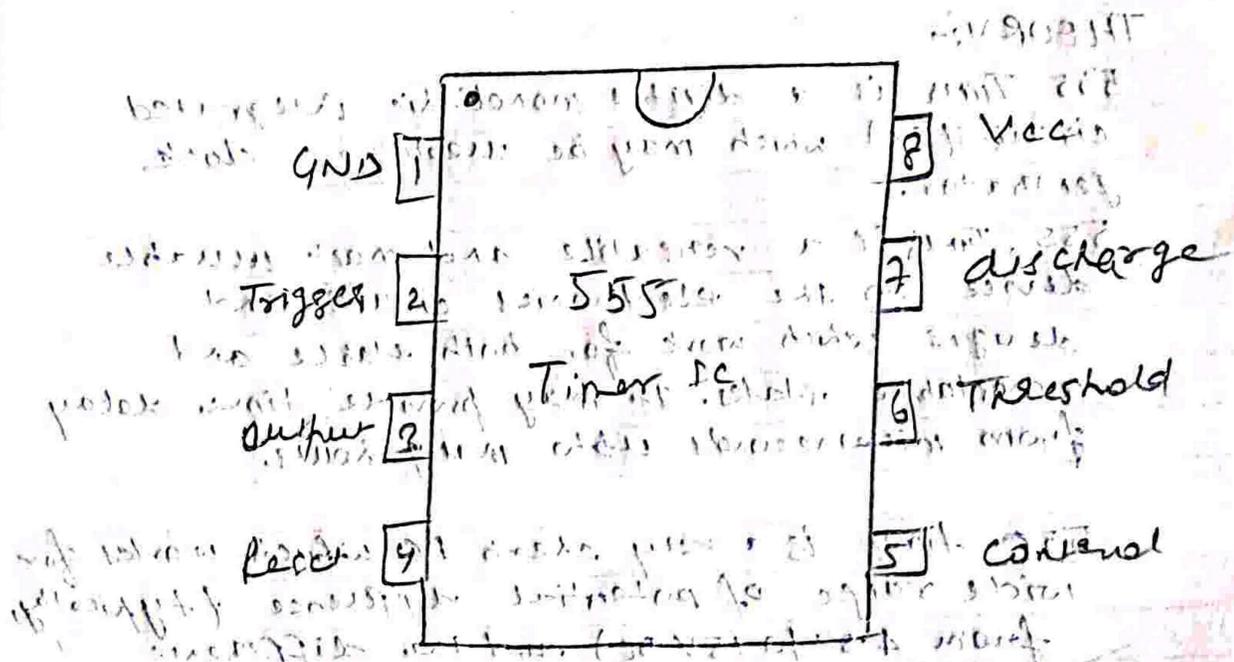
555 Timer is a digital monolithic integrated circuit (IC) which may be used as a clock generator.

555 Timer is a versatile and most valuable device in the electronics circuits and designs which work for both stable and monostable states. It may provide time delay from microseconds upto many hours.

555 timer is a very cheap IC which works for wide range of potential difference (typically from 4.5 to 15V DC) and the difference provided input voltages do not affect the timer output.

555 Timer is a ~~linear~~ linear device and it can be directly connected to the CMOS or TTL (Transistor-Transistor logic) digital circuits due to its compatibility but, interfacing is must to use 555 timer with other signal digital circuits.

# 555 Timer IC Pin Configuration



## 555 Timer IC Pin Diagram

The 555 timer IC is a monolithic integrated circuit that can be configured as an astable multivibrator, monostable multivibrator, or bistable multivibrator. It is widely used in timing applications. The pin configuration is as follows:

- Pin 1: Ground (GND)
- Pin 2: Trigger
- Pin 3: Output
- Pin 4: Vcc (Supply Voltage)
- Pin 5: Control
- Pin 6: Threshold
- Pin 7: Discharge
- Pin 8: Vcc (Supply Voltage)

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## Applications of 555 timer.

555 timer is most important integrated circuit (chip) used widely in digital electronics. Some common uses and application of 555 timer IC are as follows-

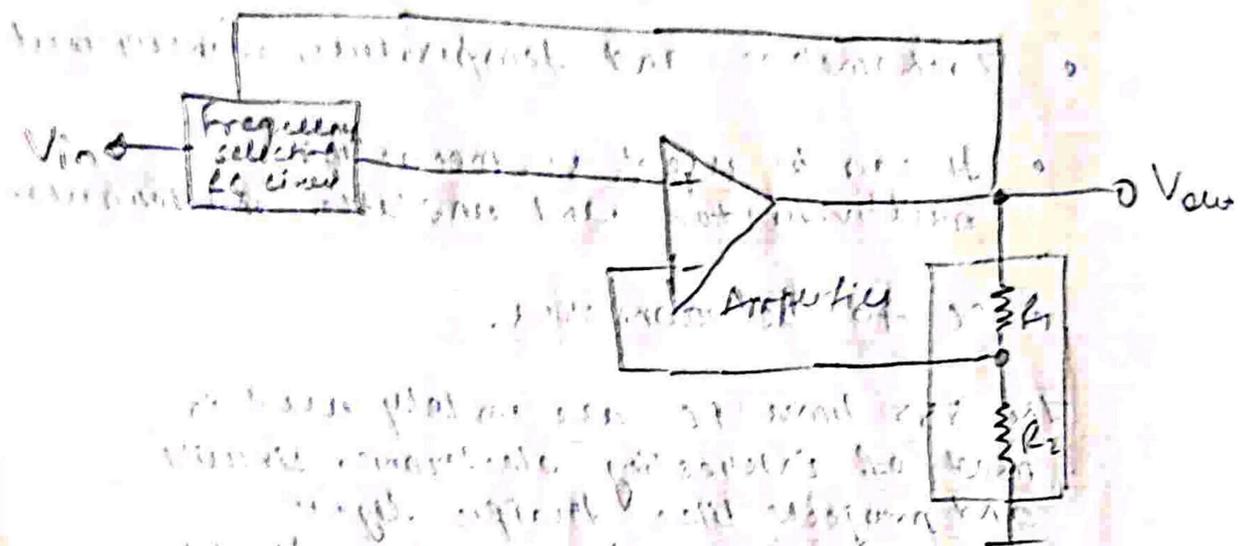
- PWM (pulse width modulation) & PPM (Pulse Position Modulation)
- Duty cycle oscillator
- Lamp timer
- To provide accurate time delays.
- As a flip-flop element
- Digital logic probes
- Analog-frequency meters
- Quad Timer Applications
- Pulse, waveform and square wave generation.

- Stepped wave and tone burst generator and linear ramp generation.
- Tachometrics and temperature measurement.
- It can be used as monostable multivibrator and unstable multivibrator.
- DC to DC converter.

The 555 timer IC are widely used in most of interesting electronic circuits and projects like traffic light circuit using 555 timer, LED flashing circuits, police siren, LED dice, Joystick and game paddles and low cost line receiver, clap switch activated circuit and lots of other projects and circuits design.

# Op-Amp

Op-Amp is used to amplify the input signal. It is a high gain differential amplifier.



Op-Amp is used to amplify the input signal. It is a high gain differential amplifier. The output of the op-amp is  $V_{out}$ . The feedback network consists of two resistors,  $R_1$  and  $R_2$ , connected between the output and the inverting input. This forms a negative feedback circuit.

## Negative feedback circuit

The negative feedback circuit is used to stabilize the gain of the op-amp. It is used to create various types of op-amp configurations such as voltage follower, inverting amplifier, and non-inverting amplifier.

AIM:- Design of Active filters.

THEORY:-

An active filter is a type of filter that includes one or more active circuit components, such as a transistor or an operational amplifier (op-amp). They derive their energy from an external source of energy and use it to increase or amplify signal output.

An op-amp has a high input impedance, a low output impedance and a voltage gain within its feedback loop arising from the mixture of the resistor.

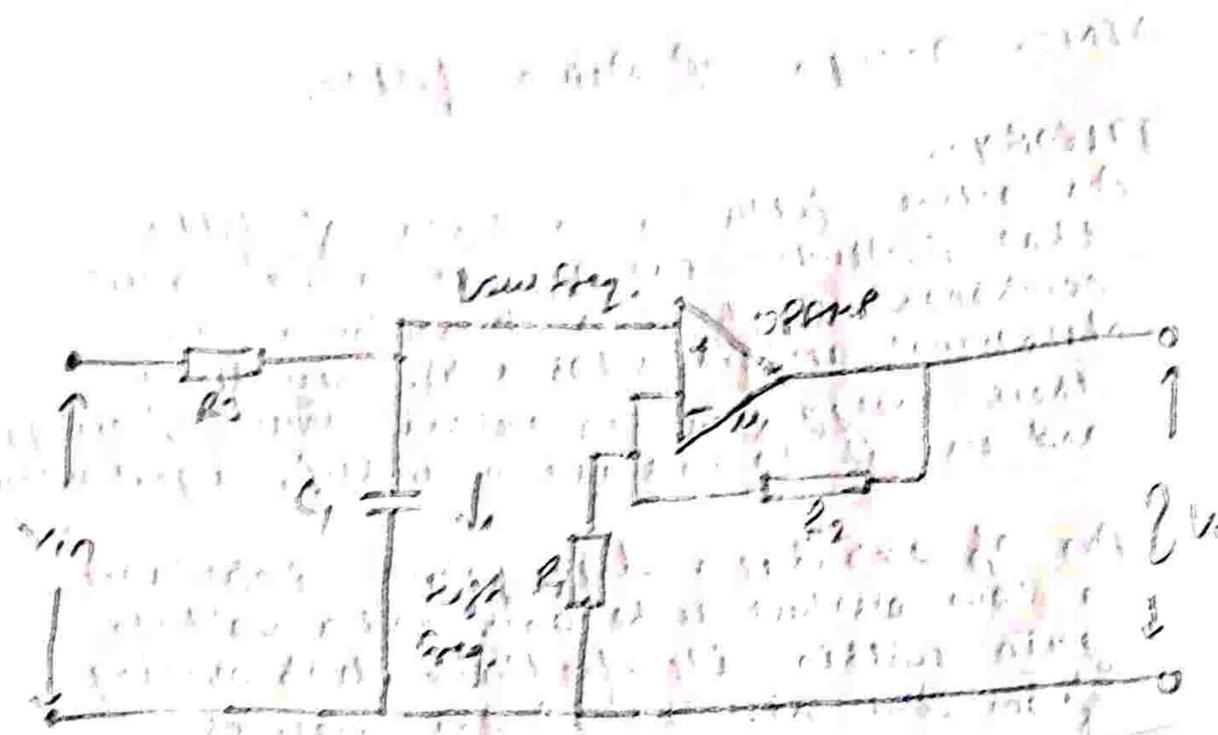
⇒ Active Low Pass filter.

The frequency response of Active low pass filter is same as that of the passive low pass filter, except the amplitude of the output signals. The voltage gain of the non-inverting operational amplifier is given as -

$$A_F = 1 + (R_2/R_1)$$

The gain of active low pass filter is given as -

$$A_V = \frac{V_{out}}{V_{in}} = \frac{A_F}{[1 + (f/f_c)^2]}$$



Active two-port folded LCR diagram

... with ...  
 ... and ...  
 ...  
 ...  
 ...  
 ...

...  
 ...  
 ...  
 ...

Where,  $A_f$  is the pass band gain  $(1 + R_2/R_1)$   
 $f$  is the frequency of output signal  
 $f_c$  is the cut off frequency.

⇒ Active High Pass Filter.

The simple Active high pass filter can be obtained by connecting a non-inverting or inverting operational amplifier to the passive high pass RC ckt.

In active high pass filter pass band is limited due to the open loop characteristics of op-amp. The gain of active high pass filter is given as -

$$A_v = V_{out}/V_{in} = \frac{A_f (f/f_c)}{\sqrt{1 - (f/f_c)^2}}$$

Where,  $A_f$  is the pass band gain  $(1 + R_2/R_1)$   
 $f$  is the frequency of input signal.  
 $f_c$  is the cut-off frequency.

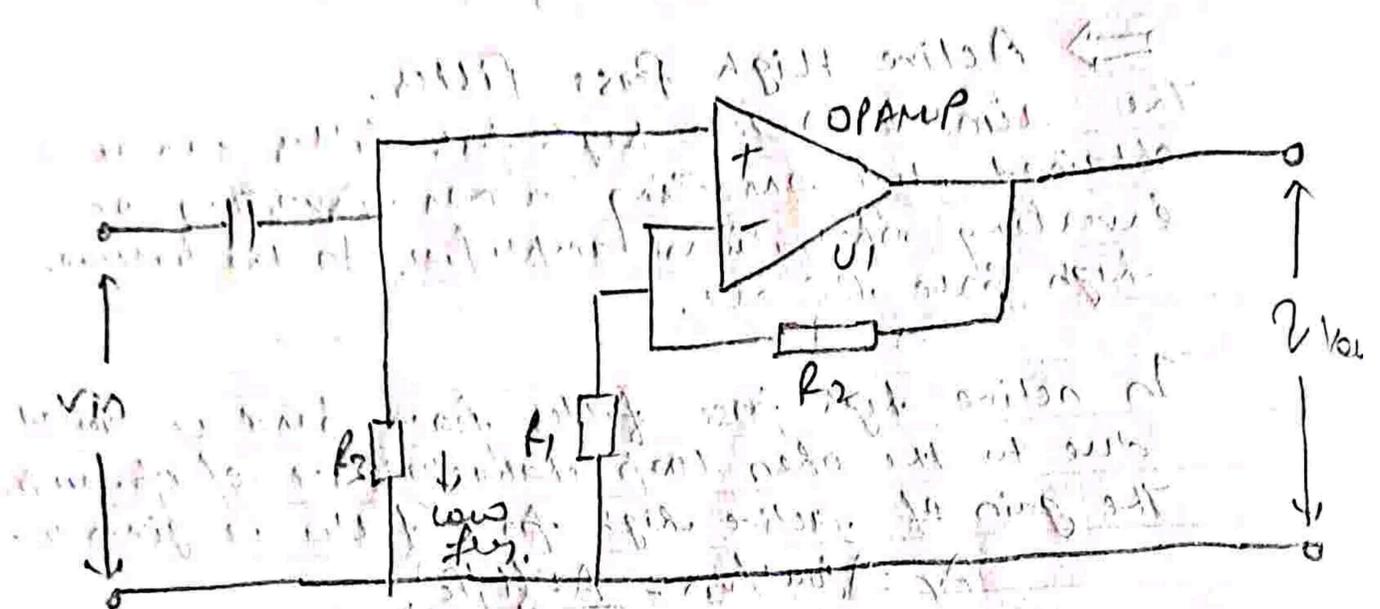
Voltage gain in dB is given as -

$$A_v (dB) = 20 \log_{10} (V_{out}/V_{in})$$

$$-3dB = 20 \log_{10} (0.707 \times V_{out}/V_{in})$$

Active High Pass Filter

Handwritten notes describing the filter's characteristics, including its frequency response and gain.



Active High Pass filter Ckt. Diagram

Handwritten notes explaining the circuit's operation and its frequency response.

Handwritten equation:  $A_v(f) = \frac{R_2}{R_1} \frac{f}{f_c}$

Handwritten notes related to the filter's gain and cutoff frequency.

## ⇒ Active Band Pass filter.

Band Pass is a filter is frequency selective filter used in electronic systems to allow a particular band or certain range of frequency. The range of frequencies is set between two cut-off frequency ( $f_c$  &  $f_H$ ).

The cascade connection of low pass filter and high pass filter produces a low "Quality factor" type filter which has wide pass band.

**AIM:-** Study and application of PLL IC.

**APPARATUS:-**

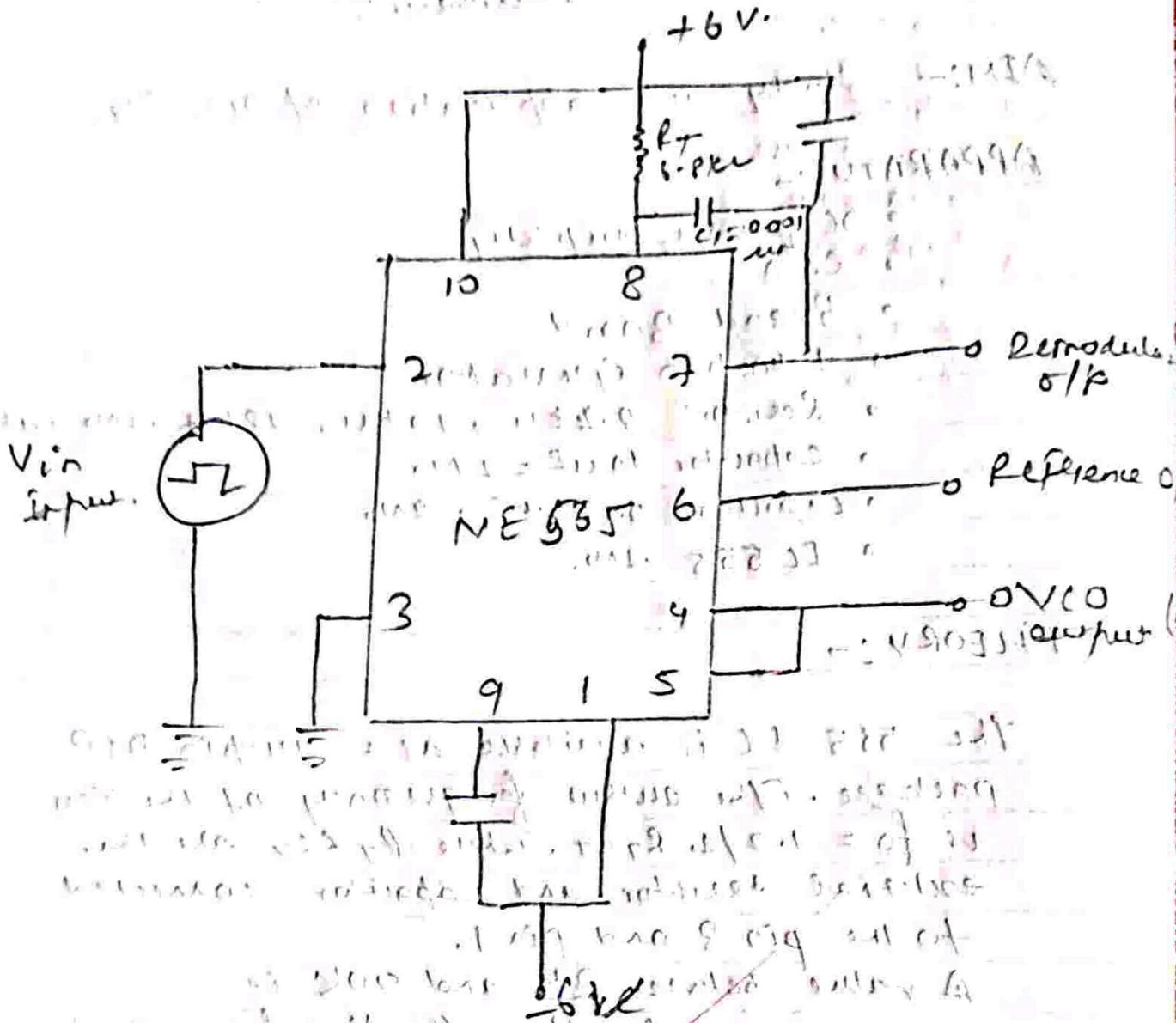
- DC power supply
- CRO
- Bread Board
- Function Generator
- Resistor  $2.2k\Omega$ ,  $10k\Omega$ ,  $18k\Omega$  - 1 No each
- Capacitor  $10\mu F = 1 No$
- Capacitor  $0.02\mu F = 2 No$
- IC 565 - 1 No.

**THEORY:-**

The 565 IC is available as a 14-pin DIP package. The output frequency of the VCO is  $f_o = 1.2 / (R_T C_T)$ , where  $R_T$  &  $C_T$  are the external resistor and capacitor connected to the pin 8 and pin 9.

A value between  $2k\Omega$  and  $20k\Omega$  is recommended for  $R_T$ . The VCO free running frequency is adjusted with  $R_T$  and  $C_T$ , so that it is not centre of the input frequency range.

# Circuit diagram:

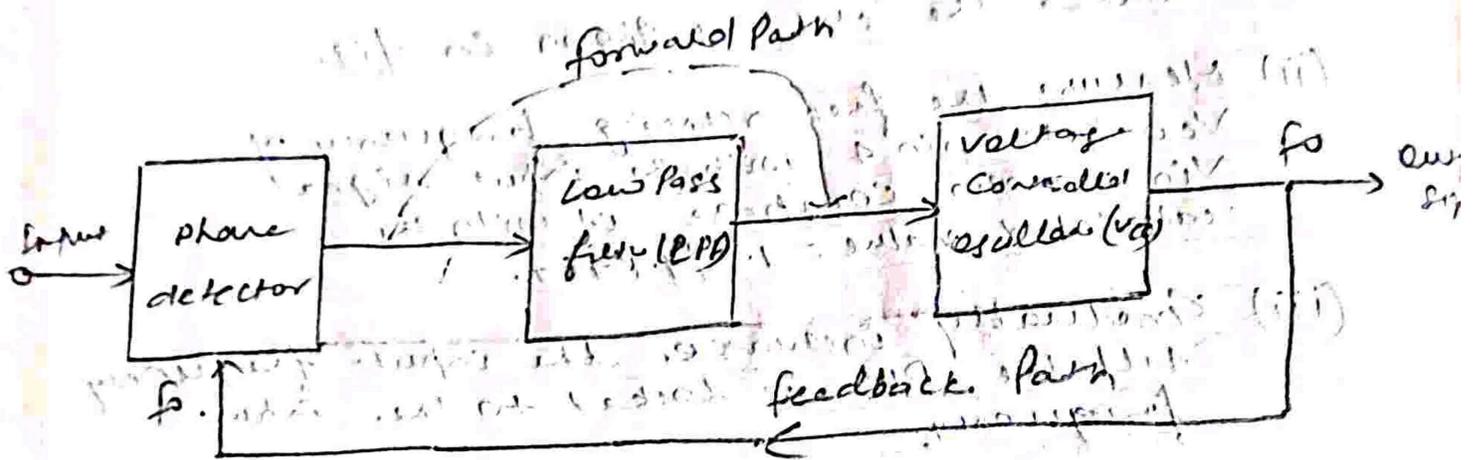


-6V

### PROCEDURE:-

- (i) Connect the circuit as shown in fig.
- (ii) Measure the free running frequency of  $V_{CO}$  at pin 4 with the input signal  $V_{in} = \text{zero}$ . Compare it with the calculated value  $= 1/2 \sqrt{4 R T C T}$ .
- (iii) Gradually increase the input frequency till the PLL is locked to the input frequency.
- (iv) This frequency  $f_{c1}$  gives the lower end of the capture range.
- (v) If the input frequency is increased further the loop will be in unlocked condition only.
- (vi) Now gradually decrease the input frequency till the PLL is again get locked. This is the frequency  $f_{c2}$ , the upper end of the capture range.  
Proceed on decreasing the input frequency

# PLL Block diagram



(i) The output of the phase detector is a voltage proportional to the phase error between the input and the feedback signal. This error signal is filtered by the LPF to produce a smooth control voltage for the VCO.

(ii) The VCO generates an output signal whose frequency is proportional to the control voltage. The output frequency is  $f_o$ .

(iii) The output signal is fed back to the phase detector through the feedback path. The feedback signal is also filtered by the LPF.

(iv) The feedback path is used to compare the phase of the output signal with the phase of the input signal. The phase detector outputs a voltage proportional to the phase error.

(v) The LPF is used to filter the output of the phase detector. The LPF has a low pass characteristic, which means that it allows low frequency signals to pass through it, but it attenuates high frequency signals.

(vi) The VCO is a voltage controlled oscillator. This means that the frequency of the output signal is controlled by the voltage applied to it. The VCO is used to generate an output signal whose frequency is proportional to the control voltage.

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until the loop is unlocked. This frequency,  $f_{LL}$  gives the lower end of the lock range.

RESULT:-

$f_0$  free running frequency.

$f_{LL}$  lower locking frequency:

$f_{CL}$  lower capture frequency:

$f_{CH}$  higher capture frequency:

$f_{LH}$  higher locking frequency:

OUTCOME:-

After conducting this experiment, students are able to understand the applications of PLL.

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Experiment 6

AIM:- Design of binary Adder and Subtractor.

THEORY:-

(Half Adder)

Half adder is a combinational logic circuit with two inputs and two outputs. The half adder ckt. is designed to add two single bit binary numbers A and B. It is the basic building block for addition of two single bit numbers. The circuit has two outputs carry and sum.

Truth Table :-

| Input |   | Output |   |
|-------|---|--------|---|
| A     | B | S      | C |
| 0     | 0 | 0      | 0 |
| 0     | 1 | 1      | 0 |
| 1     | 0 | 1      | 0 |
| 1     | 1 | 0      | 1 |

(Full Adder)

full adder is developed to overcome the drawback of Half-Adder ckt. It can add two one-bit numbers, A and B, and carry C. The full adder is a three input and two output combinational ckt.

Truth Table:

| Inputs |   |     | Outputs |    |
|--------|---|-----|---------|----|
| A      | B | Cin | S       | Co |
| 0      | 0 | 0   | 0       | 0  |
| 0      | 0 | 1   | 1       | 0  |
| 0      | 1 | 0   | 1       | 0  |
| 0      | 1 | 1   | 0       | 1  |
| 1      | 0 | 0   | 1       | 0  |
| 1      | 0 | 1   | 0       | 1  |
| 1      | 1 | 0   | 0       | 1  |
| 1      | 1 | 1   | 1       | 1  |

## (Half Subtractor)

Half subtractor is a combinational circuit with two input and two outputs.

It produces the difference between two binary bits at the input and also produces an output (Borrow). To indicate if a 1 has been borrowed. In the subtraction  $(A - B)$ , A is called as Minuend bit and B is called as Subtrahend bit.

Truth Table.

| Input |   | Output |        |
|-------|---|--------|--------|
| A     | B | (A-B)  | Borrow |
| 0     | 0 | 0      | 0      |
| 0     | 1 | 1      | 1      |
| 1     | 0 | 1      | 0      |
| 1     | 1 | 0      | 0      |

## (Full Subtractor)

The disadvantage of a half subtractor is overcome by full subtractor. The full subtractor is a combinational circuit with three inputs A, B, C and two outputs D and C'. A is the "minuend" produced by the previous stage D is the difference output and C' is the borrow output.

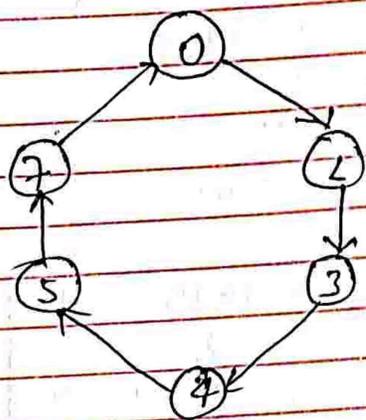
Truth Table.

| Inputs |   |   | Outputs |    |
|--------|---|---|---------|----|
| A      | B | C | (A-B-C) | C' |
| 0      | 0 | 0 | 0       | 0  |
| 0      | 0 | 1 | 1       | 1  |
| 0      | 1 | 0 | 1       | 1  |
| 0      | 1 | 1 | 0       | 1  |
| 1      | 0 | 0 | 1       | 0  |
| 1      | 0 | 1 | 0       | 0  |
| 1      | 1 | 0 | 0       | 0  |
| 1      | 1 | 1 | 1       | 1  |

AIM:- Design of Counter.

Problem :- Design synchronous counter for sequence:  $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 0$ , using T-flip-flop.

Explanation:- for given sequence, state transition diagram as following below



State transition table logic -

| Present State | Next state |
|---------------|------------|
| 0             | 1          |
| 1             | 2          |
| 2             | 3          |
| 3             | 4          |
| 4             | 5          |
| 5             | 6          |
| 6             | 0          |

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Experiment 7

State transition table for given sequence

| Present state |       |       |            | Next state |            |
|---------------|-------|-------|------------|------------|------------|
| $Q_3$         | $Q_2$ | $Q_1$ | $Q_3(t+1)$ | $Q_2(t+1)$ | $Q_1(t+1)$ |
| 0             | 0     | 0     | 0          | 0          | 1          |
| 0             | 0     | 1     | 0          | 1          | 1          |
| 0             | 1     | 1     | 1          | 0          | 0          |
| 1             | 0     | 0     | 1          | 0          | 1          |
| 1             | 0     | 1     | 1          | 1          | 1          |
| 1             | 1     | 1     | 0          | 0          | 0          |

T flip-flop :- If value of  $Q$  changes either from 0 to 1 or from 1 to 0 then input for T flip-flop is the input value is 1.

| $Q_t$ | $Q_{t+1}$ | T |
|-------|-----------|---|
| 0     | 0         | 0 |
| 0     | 1         | 1 |
| 1     | 0         | 1 |
| 1     | 1         | 0 |

Input Table of flip-flops.

| $T_3$ | $T_2$ | $T_1$ |
|-------|-------|-------|
| 0     | 0     | L     |
| 0     | L     | 0     |
| 1     | L     | L     |
| 0     | 0     | L     |
| 0     | L     | 0     |
| 1     | L     | L     |

find value of  $T_3, T_2, T_1$  in terms of  $Q_3, Q_2, Q_1$  using k-map (Karnaugh Map).

| $T_3$         | 00 | 01 | 11 | 10 |
|---------------|----|----|----|----|
| $Q_3/Q_2/Q_1$ |    |    |    |    |
| 0             | 0  | 0  | 1  | X  |
| L             | 0  | 0  | L  | X  |

Therefore,  
 $T_3 = Q_2$ .

| $T_2$         | 00 | 01 | 11 | 10 |
|---------------|----|----|----|----|
| $Q_3/Q_2/Q_1$ |    |    |    |    |
| 0             | 0  | L  | L  | X  |
| L             | 0  | L  | L  | X  |

Therefore,  $T_2 = Q_2$

| $T_2$ | 00 | 01 | 11 | 10 |
|-------|----|----|----|----|
| 0     | 1  | 1  | 0  | 1  |
| 1     | 1  | 1  | 0  | 1  |

Therefore,  
 $T_1 = Q_2$

Now, you can design required circuit using expressions of k-maps.

AIM:- Study of Multiplexer and demultiplexer / decoder.

THEORY:-

### (MULTIPLEXER)

Multiplexer means many into one. A multiplexer is circuit used to select and route any one of the several input signals to a single output. A simple example is a single pole multi-throw switch.

Multiplexer can handle two type of data.  
i.e Analog and Digital.

for analog application, multiplexers are built using relays and transistor switches.

for digital application they are built from standard logic gates.

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Experiment 8

The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many inputs but only one output.

By applying control signals (also known as select signals), we can steer any input to the output.

Some of the common types of multiplexers are 2-to-1, 4-to-1, 8-to-1 and 16-to-1 etc. multiplexers.

### Application of multiplexers.

Multiplexers are used in various fields where multiple data need to be transmitted using a single line.

Following are some of the applications of multiplexers.

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Supplement - 8

### • Communication System -

It is a set of system that enable communication like transmission system, relay and Tributary station and communication network.

### • Telephone Network -

In telephone network, multiple audio signals are integrated on a single for transmission with the help of multiplexers.

### • Computer Memory :-

Multiplexers are used to implement huge amount of memory into the computer and the same time reduces the number of copper lines required to connect the other parts of computer.

### • Transmission from the computer system of a satellite -

Multiplexers can be used for the transmission of data signals from the computer system of a satellite or spacecraft, etc.

## (DEMULTIPLEXER.)

Demultiplexer means one to many. A demultiplexer is a circuit with one input and many outputs.

By applying control signal, we can steer any input to the outputs.

Ex. of demultiplexer are 1 to 2, 1 to 4, 1 to 8, 1 to 16 etc.

### Applications of demultiplexer.

It is used to connect a single source to multiple destinations.

The main applications area of demultiplexer is communication system, where multiplexers are used.

Most of the communication systems are bidirectional (i.e. they function in both ways: transmitting and receiving signals).

Hence, for most of the applications, the multiplexers work in syn.

demultiplexers are also used for reconstruction of parallel data and ALU circuits.

AIM:- Implementation of combinational logic circuits.

### THEORY:-

The implementation of boolean function using decoders was already discussed in the experiment 5.

The same approach is applicable in the using ROM, since ROM is the device that includes both a decoder and OR gates within the same chip.

The blowing off of appropriate fuses or opening the links is referred to as programming.

The designer needs only to specify a ROM program table that provides information for the required pairs in the ROM.

Example: Find the squares of 3-bit Number.

Solution: This example has already discussed and implemented with the classical method in chapter 5.

There are 3 input variables and six output functions.

To implement with ROM a  $2^3 \times 6$  ROM or  $8 \times 6$  ROM is required.

| Decimal | X Y Z | Decimal | A | B | C | D | E | F |
|---------|-------|---------|---|---|---|---|---|---|
| 0       | 0 0 0 | 0       | 0 | 0 | 0 | 0 | 0 | 0 |
| 1       | 0 0 1 | 1       | 0 | 0 | 0 | 0 | 0 | 1 |
| 2       | 0 1 0 | 4       | 0 | 0 | 0 | 1 | 0 | 0 |
| 3       | 0 1 1 | 9       | 0 | 0 | 1 | 0 | 0 | 1 |
| 4       | 1 0 0 | 16      | 0 | 1 | 0 | 0 | 0 | 0 |
| 5       | 1 0 1 | 25      | 0 | 1 | 1 | 0 | 0 | 1 |
| 6       | 1 1 0 | 36      | 1 | 0 | 0 | 1 | 0 | 0 |
| 7       | 1 1 1 | 49      | 1 | 1 | 0 | 0 | 0 | 1 |

AIM:- Study of DAC and ADC

Background:-

Digital-to-Analog converters (DACs) and analog-to-digital converters (ADC) are important building blocks which interface sensors (eg. temperature, pressure, light, sound, counting speed or cal) to digital systems such as microcontrollers or PCs.

(Digital to Analog converter)

Addition of digital inputs (Dart) where say  $i$  corresponds to 5 volt give rise to analog output, which can be added with different weights considering their place in binary number. But this type of circuit has a disadvantage of requirement of large number of accurate resistors for high number of bits. eg. 8 bit converter require eight resistor varying from some value  $R$  to  $128R$ .

## (Analog-to-digital converter)

Analog to digital converter is for conversion of analog input (any physical quantity such as temp) to digital output in binary form. (which can be read by computer) and further it can be converted to binary decimal format.

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